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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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JONATHAN T. KAPLAN
ATTORNEY AT LAW
140 NASSAU STREET
NEW YORK, NY 10038-1501

EXAMINER	
ROSALES HANNER, MORELLA I	
ART UNIT	**PAPER NUMBER**
2128	10

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/660,026	CHOWDHURY ET AL.	
	Examiner	Art Unit	
	Morella I Rosales-Hanner	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 September 0200*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 September 0200* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. **Claims 1 – 21** have been examined and are pending.

Specification

2. The specification portion of this application contains an appendix [**Appendix A pages 1 – 10**] listing Tag Propagation Model for various Verilog constructs. Applicant may bodily incorporate the 10 pages now denoted as Appendix or it may be submitted as a compact disc conforming to the standards set forth in **37 CFR 1.96(c)(2)** and must be appropriately referenced in the specification (see **37 CFR 1.77(b)(4)**). Alternately, applicant may submit denoted Appendix A. If the denoted Appendix A is submitted as drawings, it must be submitted in the manner and complying with the requirements for drawings as provided in **§1.84**. At least one figure numeral is required on each sheet of drawing.

3. The disclosure is objected to because of the following informalities found in page 13, line 27:

... wherein the Monitoring Process 106 is a typically a program...

It appears that it should recite:

... wherein the Monitoring Process 106 is typically a program.

Appropriate correction is required.

Drawings

4. Formal drawings are required in response to this Office action. A proposed drawing correction or corrected drawings are required in reply to the Office action to

avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim objections

5. **Claim 21** is objected to because of the following informalities: the claim contains multiple transitional phases. This claim recites

"...A computer program product ***comprising*** *a computer usable medium having computer readable code embodied therein, the computer program product* ***comprising****:..."*

Appropriate correction is required.

Possible Allowable Subject Matter

6. **Independent claims 1, 20 and 21** may be allowable if rewritten or amended to overcome the rejections over prior art of record. The prior art of record does not expressly teach the specific details of the following:

- definition of a Tag Value as well as the elements that comprised a tag value such as "tag ID" [**as defined and taught at page 5, lines 10 –12 of the specification**], "tag history" [**as defined and taught at page 5, lines 16 – 23 of the specification**], "tag last used" [**as defined and taught at page 5, lines 25 – 30 of the specification**], and

- definition of what an assignment statement is as well as the elements that comprise an assignment statement.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Examiner has applied the Graham v. Deere test for determining obviousness as follows:

(A) Determining the scope and contents of the prior art;

(B) Ascertaining the differences between the prior art and the claims in issue;

(C) Resolving the level of ordinary skill in the pertinent art; and

(D) Evaluating evidence of secondary considerations.

7.1. Claims 1 – 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over **U.S Patent No. 6,141,630** issued to McNamara et al., hereafter referred to as *McNamara* in view of a printed publication by Grinwald et al. titled "**User Defined Coverage**

– A Tool Supported Methodology for Design Verification" dated June 1998 hereafter referred to as *Grinwald*, in further view of **US Patent No. 6,053,947** issued to Dale Parson, hereafter referred to as *Parson*.

7.1.1 As regard to **independent claim 1,** this claim is drawn to a method performed by a data processing system having a memory, comprising the steps of:

- simulating HDL "assignment statements" to determine a logical value for a target signal for a set of input values.
- identifying input signals (subset) having effect on a target signal value based upon values of input signals and interrelation; and
- determining a tag value for a signal comprising an identifier of the assignment statement and a history comprised of a propagation of a tag value of each input signal that is a member of the subset of input signals.

McNamara teaches:

- simulating test vectors to determine logical values for a target signal for a set of input values **[Fig. 1 and accompanied text]**;
- determining (identifying) sequence of actions variables that need to be set or what condition needs to occur (input signals) to activate targeted arcs, blocks or paths from a given state (interrelation) **[Col 4, lines 46 – 57]**

McNamara fails to expressly teach the use of assignment statements during the HDL simulation that is well know in the art as being inherited to a design language such as Verilog or VHDL. *McNamara* also fails to expressly teach determining information that identifies assignment statement as well as signal propagation history.

Grinwald teaches the use of event traces, **[Pg 161, section 4.2]** to determine if a coverage task (Target signal) was executed during a test, which provide information such as instruction name, instruction order, interrupt basis, etc. *Grinwald* further teaches **[Pg 158, Introduction section]** that the main disadvantage of code coverage tools is that they don't "understand" the application domain making it hard to tune the tools to areas which the user thinks are of significant

Parson teaches **[Col 10, Bus Signal section]** the use of tags that are provided to support dataflow, more specifically to connect input and output signals values. *Parson* further teaches **[Col 1, lines 45 – 54]** that circuit modelers are limited to data formats and run-time signal propagation strategies hard coded into the simulation engines usually resulting in hand coding when verifying no-traditional circuits.

Therefore, it would have been obvious to one of ordinary skills in the art, at the time of the invention to combine the use event traces to determine if a coverage task (target signal) was executed as taught by *Grinwald* and the use of tag values, to automatically determined data flow information associated with input and output signals, as taught by *Parson* with the method taught by *McNamara* in order to aid circuit designer proceed towards circuit manufacturing with confidence by providing customizable data formats and automatic run-time signal propagation information.

7.1.2. **Claims 2 and 3** are drawn to:

- identifying a second subset of a set of input signals to a conditional statement of the HDL specification having an observably controllable effect upon whether the assignment statement is simulated and satisfied, membership in the second subset being based upon a logical value for each of an input signal to the conditional statement and a functional interrelation of the input signals to the conditional statement; and
- determining history to be additionally comprised of a propagation of a tag value of each signal of the second subset.

McNamara teaches **[Fig. 4 and accompanied text]** a method of identifying subsets of a set of test vectors representing input signals to a conditional statement of the HDL specification in order to test basic block, transition arcs (conditional statements) and path of interest (observation points). *McNamara* fails to expressly teach determining tag history to capture signal propagation information.

Grinwald teaches **[section 4.2, last paragraph]** the use of trace data to determine the list of task that occurred in a test. *Grinwald* also teaches, for reporting analysis purposes, trace data for each task such as first and last time each task occurred.

Parson teaches **[Code block 9 and accompanied text]** the use of an audit feature to log signal propagation history.

It would have been obvious to one of ordinary skills in the art, at the time of the invention, to combine the step of determining the list of tasks that occurred in a test as taught by *Grinwald* and the audit feature as taught by *Parson* with the method taught by *McNamara* in order to provide signal propagation history information that can be used for analysis purposes.

7.1.3 **Claims 4, 5 and 6** are drawn to creating a copy of a tag value.

McNamara teaches **[Fig 2 and accompanied text]** an output log database that stores output from the simulated design for later analysis by other electronic design automation tools. *McNamara* fails to expressly teach output from the simulated design to the output log database that include assignment statements for logical signals values associated with a target signal.

Grinwald teaches **[Fig. 5 and accompanied text]** a list of attributes such as interrupts basic and instruction groups that are copied into an event trace table in order to detect the list of tasks that occurred during a given test. *Grinwald* further teaches **[section 4.3, paragraph 1]** that the most direct way in which coverage testing can assist the verification process is by detecting illegal events and that detection of illegal events can be difficult, since they may consist of a series of sub-events, each occurring in different parts of the design or at different times.

Parson teaches **[code block 9 and accompanied text]** a signal audit feature capable of capturing detailed signal propagation information.

It would have been obvious to one of ordinary skills in the art, at the time of the invention, to store the list of tasks that occurred during a given test and signal

propagation information as taught by *Grinwald* and *Parson* as part of the output log database taught by *McNamara* in order to assist in the detection of illegal events.

7.1.4. **Claims 7, 8, 9 - 14** are drawn to propagation of logical values for target signals, within a module instantiation comprising the assignment statement, to a higher-level signal of the HDL specification.

McNamara teaches **[Fig 1 and related text]** the identification of what variables need to be set and what conditions need to be met so that the simulated design transitions to an untested state from a currently active state. *McNamara* also teaches the approach of determining what sequence of actions to take in order to activate targeted arcs, blocks, or paths from the given state of the design. *McNamara* further teaches that conditions that need to occur are typically defined in terms of some timing constraint.

McNamara fails to expressly teach propagation of target values from target signals within a module instantiation.

Grinwald teaches **[section 4.2, Pg 162]** detection of a list of tasks that occurred in a test and reporting of any illegal tasks in order to improve the verification process.

Parson teaches **[code block 9 and accompanied text]** a signal audit feature capable of capturing detailed signal propagation information performed by the model generator module during construction (instantiation) and that this information is captured to assure design integrity.

It would have been obvious to one of ordinary skills in the art, at the time of the invention, to store the list of tasks that occurred during a given test and signal

propagation information during construction (instantiation) time as taught by *Grinwald* and *Parson* as part of the output log database taught by *McNamara* in order to improve the verification process and assure design integrity.

7.1.5 **Claims 15 - 19** are drawn to determining whether a flipping of a first logical value of the first input signal will cause a flipping of the logical value of the target signal.

McNamara teaches **[Col 4, lines 4 – 36]** the automatic construction (determination) of a set of test vectors (logical values) for causing each state of a state machine to be visited and each transition arc to be taken in order to prove whether each of the basic blocks that make up the design description are correct. *McNamara* also teaches producing another set of test vectors for proving that user-selected subsets of the basic blocks work together correctly.

McNamara fails to expressly teach that the above determination of test vectors is directed to a first logical value associated with a first input signal

Grinwald teaches **[section 4.1.1]** that it is important to test all possible pairs of instructions with all types of interrupts between then since incomplete or wrong cleanup after interrupts is a source of many bugs.

Parson teaches **[Col 5, lines 4 –12]** a process of simulating a circuit that comprises distributing an input signal only upon a change in the signal, and then only to those simulation models that use the signal. The signal, therefore, is only distributed to those functions that use it, as opposed to traditional netlist simulation models where signal values are pass up and down the hierarchy during simulation.

It would have been obvious to one of ordinary skills in the art, at the time of the invention, to determine possible combination of signals as taught by *Grinwald* and distribute the input signals only upon a change in the signal to those functions that use the signals as taught by *Parson* as part of the process of automatic determination of test vectors as taught by *McNamara* in order to improve traditional netlist simulation models.

7.1.6. **Claim 20** is drawn to a data processing system having a memory, comprising:

- a sub-system for simulating HDL "assignment statements" to determine a logical value for a target signal for a set of input values,
- a sub-system for identifying input signals (subset) having effect on a target signal value based upon values of input signals and interrelation; and
- a sub-system for determining a tag value for a signal comprising an identifier of the assignment statement and a history comprised of a propagation of a tag value of each input signal that is a member of the subset of input signals.

McNamara teaches a system for automated design verification comprising:

- a sub-system for simulating test vectors to determine logical values for a target signal for a set of input values **[Fig. 1, element 112 and accompanied text]**; and

- a sub-system for determining (identifying) sequence of actions variables that need to be set or what condition needs to occur (input signals) to activate targeted arcs, blocks or paths from a given state (interrelation) **[Col 4, lines 46 – 57]**

McNamara fails to expressly teach the use of assignment statements during the HDL simulation which is well know in the art, as being inherited to a design language such as Verilog or VHDL. *McNamara* also fails to expressly teach a sub-system for determining information that identifies assignment statement as well as signal propagation history.

Grinwald teaches a sub-system that uses event traces **[Pg 161, section 4.2]** to determine if a coverage task (Target signal) was executed during a test and that provides information such as instruction name, instruction order, interrupt basis, etc,.

Parson teaches **[Col 10, Bus Signal section]** a simulation model sub-system that uses tags to support dataflow, more specifically to connect input and output signals values. *Parson* further teaches **[Col 3, lines 59 – 62]** a system that renders the construction simulation models straightforward for circuit designers and facilitates automatic generation of circuit simulation models since many existing circuit capture and synthesis tools and methodologies deliver their output in the form of hierarchical netlist.

Therefore, it would have been obvious to one of ordinary skills in the art, at the time of the invention to include a sub-system for determining if a coverage task (target signal) was executed during a test as taught by *Grinwald* a long with a sub-

system that uses tag values to automatically determined data flow information associated with input and output signals as taught by *Parson* as part of the system disclosed by *McNamara* in order to aid circuit designer generate straightforward simulation models that deliver user friendly output.

7.1.7 **Claim 21** is drawn to a computer program product comprising a computer usable medium having computer readable code embodied therein, the computer program product comprising computer readable program code devices configured to cause a computer to effect:

- simulating HDL "assignment statements" to determine a logical value for a target signal for a set of input values,
- identifying input signals (subset) having effect on a target signal value based upon values of input signals and interrelation; and
- determining a tag value for a signal comprising an identifier of the assignment statement and a history comprised of a propagation of a tag value of each input signal that is a member of the subset of input signals.

McNamara teaches a computer program on a computer readable medium that is executed on a computer to:

- simulate test vectors to determine logical values for a target signal for a set of input values **[Fig. 1, element 112 and accompanied text]**; and

- determine (identify) sequence of actions variables that need to be set or what condition needs to occur (input signals) to activate targeted arcs, blocks or paths from a given state (interrelation) **[Col 4, lines 46 – 57]**

McNamara fails to expressly teach the use of assignment statements during the HDL simulation which is well know in the art, as being inherited to a design language such as Verilog or VHDL. *McNamara* also fails to expressly teach determining information that identifies assignment statement as well as signal propagation history.

Grinwald a computer program on a computer readable medium that is executed on a computer that uses event traces **[Pg 161, section 4.2]** to determine if a coverage task (Target signal) was executed during a test and that provides information such as instruction name, instruction order, interrupt basis, etc.

Parson teaches **[Col 10, Bus Signal section]** a computer program, on a computer readable medium that is executed on a computer, which uses tags to support dataflow, more specifically to connect input and output signals values. *Parson* further teaches **[Col 3, lines 59 – 62]** a computer program that renders the construction simulation models straightforward for circuit designers and facilitates automatic generation of circuit simulation models since many existing circuit capture and synthesis tools and methodologies deliver their output in the form of hierarchical netlist.

Therefore, it would have been obvious to one of ordinary skills in the art, at the time of the invention to combine the computer program product disclosed by *McNamara* with computer readable code configured to determine if a coverage task

(target signal) was executed during a test as taught by *Grinwald* a long with a computer program product that uses tag values to automatically determined data flow information associated with input and output signals as taught by *Parson* in order to aid circuit designer generate straightforward simulation models that deliver user friendly output as taught by *Parson*.

Remarks

8. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- US Patent No. 5,553,002 issued to Dangelo et al.,
- US Patent No. 5,870,588 issued to Rompaey et al.,
- US Patent No. 5,724,504 issued to Aharon et al.,
- US Patent No. 5,600,579 issued to Steinmetz, Jr.,
- US Patent No. 5,740,086 issued to Yoshio Komoto

- Ho, R.C.; Han Yang, C.; Horowitz, M.A.; Dill, D.L., "**Architecture validation for processors**" Computer Architecture, 1995. Proceedings. 22nd Annual International Symposium on, 22-24 June 1995 Pages: 404 – 413

- Grinwald, R.; Harel, E.; Orgad, M.; Ur, S.; Ziv, A., "**User defined coverage-a tool supported methodology for design verification**" Design Automation Conference, 1998. Proceedings, 15-19 June 1998 Pages: 158 - 163

- Raghavan, R.; Baumgartner, J., "**CoveT: a coverage tracker for collision events in system verification**" Performance, Computing and Communications, 1998. IPCCC '98, IEEE International, 16-18 Feb. 1998 Pages: 172 - 177

- Moundanos, D.; Abraham, J.A.; Hoskote, Y.V., "**Abstraction techniques for validation coverage analysis and test generation**" Computers, IEEE Transactions on, Volume: 47, Issue: 1, Jan. 1998 Pages: 2 - 14

- Dawson, C.; Pattanam, S.K.; Roberts, D., "**The Verilog Procedural Interface for the Verilog Hardware Description Language**" Verilog HDL Conference, 1996. Proceedings, 1996 IEEE International, 26-28 Feb. 1996 Pages: 17 – 23

- The following web pages from TransEDA:

http://web.archive.org/web/19990225100008/http://www.transeda.com/products/indexl.html

http://web.archive.org/web/19990127151441/http://www.transeda.com/products/vs_detail.html

http://web.archive.org/web/19990420103520/http://www.transeda.com/products/vs_state.html

http://web.archive.org/web/19980702103732/http://www.transeda.com/products/vs_branch.html

http://web.archive.org/web/19990420070435/http://www.transeda.com/products/vs_cond.html

http://web.archive.org/web/19990420101614/http://www.transeda.com/products/vs_path.html

http://web.archive.org/web/19990420122133/http://www.transeda.com/products/vs_trace.html

http://web.archive.org/web/19990420113203/http://www.transeda.com/products/vs_togg.html

http://web.archive.org/web/19990420092512/http://www.transeda.com/products/vs_gui.html

9. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Morella Rosales-Hanner whose telephone number is (703) 305-8883. The examiner can normally be reached Monday-Friday from 7:00 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

MRH

Mar. 31, 2004

W. Thomson
A.U. 2123
Primary Examiner